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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,729	03/30/2004	Kha H. Nguyen	02453.0029.NPUS00	8796
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HOWREY LLP-CA C/O IP DOCKETING DEPARTMENT 2941 FAIRVIEW PARK DRIVE, SUITE 200 FALLS CHURCH, VA 22042-2924			WONG, XAVIER S	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,729	NGUYEN ET AL.	
	Examiner	Art Unit	
	Xavier Szewai Wong	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30th November 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-59 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-59 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 30th November 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>11-08-04, 07-05-08</u> . | 6) <input checked="" type="checkbox"/> Other: <u>NPL search notes</u> . |

DETAILED ACTION

Information Disclosure Statement

The information disclosure statements submitted on 8th November 2004 and 5th July 2007 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

Claims 2, 28 and 56 are objected to because: please define acronyms VPRI, EXP and IPToS, e.g. Multiprotocol Label Switching (MPLS) Exponent (EXP). Appropriate correction is required.

Claims 11 and 35 are objected to because: please define acronyms PST, VST, MPLS and IPToS, e.g. Virtual State Table (VST). Appropriate correction is required.

Claim 12 is objected to because of the following informalities: line 2, add -- consists of -- before "three quality of service indicators." Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 5, 7, 8, 10, 14, 15, 22, 23, 24, 26, 55, 57, 58 and 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Maher, III et al (US 6381242 B1, "Maher").

Claims 1 and 55: Maher teaches a system for data packet marking (col. 5 lines 38-41), the system comprising:

a first memory element (fig. 2: RAM 106) wherein the first memory element is configured to receive a plurality of first packet QoS indicators (col. 5 line 51: OC-3, OC-12 and OC-48; col. 5 lines 63-66: type or protocol), a first packet QoS field (col. 5 line 67: routing information) and a second packet QoS field (col. 6 lines 8-19 → col. 8 lines 56-65: session IDs);

a second memory element (fig. 2: RAM 112) wherein the second memory element is configured to hold a plurality of second packet QoS indicators (col. 6 lines 10-13: QoS; col. 6 line 65 – col. 7 line 2: state information);

a processor (fig. 2: QoS Processor 116) configured to receive one or more QoS commands (col. 7 lines 7-11: conclusions), wherein the one or more QoS commands, includes a plurality of third QoS indicators (col. 10 lines 1-5, 20-21 & 48-51: signatures),

where the processor is configured to use an index (col. 9 lines 16-19: linked list) to search the second memory element (col. 9 lines 19-20: RAM 112), where the search is configured to return a subset of the plurality of the second QoS indicators (col. 9 lines 62-65: state of traffic flow),

where the index *may* be the first packet QoS field or the second packet QoS field (col. 6 lines 39-46: header information *may* be IP header starting byte; col. 9 lines 13-16: session ID),

where the processor is configured to create a modified data packet by determining which packet QoS fields to insert in the data packet (col. 7 line 64 – col. 8 line

6), where the determination is based on the based on the one or more QoS commands (col. 10 lines 14-20; col. 11 lines 8-14; col. 7 lines 7-17: conclusion → modification).

Claims 3 and 57, applied to claims 1 and 55: Maher further mentions the first QoS field (e.g. protocol) is used for packet modification purposes (col. 7 line 66 – col. 8 line 2), therefore, the first QoS field is read as a mark select (e.g. based on protocol) field.

Claims 4 and 58, applied to claims 1 and 55: Maher further mentions the second QoS field (session ID) is a queue number (e.g. session ID for flow queue) field (col. 8 lines 56-65; col. 9 lines 13-16).

Claim 5, applied to claim 1: Maher further mentions the first QoS field is generated by receive components (e.g. header processor 104) of a data distribution system (col. 6 lines 8-12).

Claim 7, applied to claim 1: Maher discloses the mark set generated by receive components (e.g. header processor 104; col. 5 line 63 – col. 6 line 13) of a data packet distribution system and is passed to transmit components (e.g. QoS processor 116; col. 7 line 64 – col. 8 line 2) of the data packet distribution system after the egress mark set is returned from an internal network (col. 6 lines 39-46: from internal content processor – col. 8 lines 2-6: to packet modification engine to PHY output/egress).

Claim 8, applied to claim 1: Maher teaches mark set is generated by receive components (e.g. header processor 104; col. 5 line 63 – col. 6 line 13), where addresses for the memory element are configured to correspond to the result of a search of a CAM element (col. 8 lines 56-59: CAM stores session ID which corresponds to a flow based on

addresses: col. 6 lines 20-26), and where the search of the CAM element search is based on the structure of an incoming packet (col. 6 lines 14-19: attributes).

Claim 10, applied to claim 1: Maher further teaches mark set provided by a port state table (col. 7 lines 52-59: control port manager).

Claim 14, applied to claim 1: Maher further discloses the second QoS field is a queue number generated by a distributor (col. 8 lines 56-65; col. 9 lines 13-16; e.g. session ID for flow queue), where the distributor houses a data packet receiver and transmitter (fig. 2: QoS processor).

Claim 15, applied to claim 1: Maher further discloses the one or more QoS commands are included in a transmission modification recipe (col. 7 lines 7-11: conclusions → col. 7 line 64 – col. 8 line 6).

Claim 59, applied to claim 55: Maher further mentions QoS commands generated based on incoming data package (col. 5 lines 63-65: scanning received packets) and status of transmit components (col. 6 line 65 – col. 7 line 2: content processor) that generates the commands (col. 7 lines 7-11: conclusions).

Claim 22: Maher shows a method for processing a packet (abstract) comprising: providing a multi-dimensional QoS indicator for a packet (col. 5 lines 63-66: identifying type or protocol); and selectively modifying one or more QoS fields within the packet or a packet derived there-from (col. 7 lines 64-66), responsive to at least a portion of the multi-dimensional QoS indicator (col. 7 line 66 – col. 8 line 4: based on the required protocol).

Claim 23, applied to claim 22: Maher further discloses an ingress QoS indicator (col. 5 lines 63-66: type or protocol), an egress QoS indicator (col. 6 lines 59-63: signature), and packet marking control information (col. 7 lines 7-11: conclusion), and the selective modifying step comprises selectively modifying one or more QoS fields within the packet responsive to the packet marking control information (col. 7 lines 11-17; col. 7 line 64 – col. 8 line 6: packet modification engine).

Claim 24, applied to claim 22: Maher further discloses a host QoS indicator (col. 3 lines 14-18).

Claim 26, applied to claim 22: Maher further shows utilizing egress QoS indicator as egress queue select (col. 8 lines 47-59: map session IDs to queue flows).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Claims 2, 9, 11, 16-18, 28-35, 43-47, 50-53 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, "Maher") in view of Alam (US 7340535 B1).

Claim 28: Maher teaches a system for data packet marking (col. 5 lines 38-41), wherein a first QoS field (e.g. protocol) is used for packet modification purposes (col. 7 line 66 – col. 8 line 2), therefore, the first QoS field is read as a mark set (e.g. based on protocol) field and a second QoS field (session ID) is a queue number (e.g. session ID for flow queue) field (col. 8 lines 56-65; col. 9 lines 13-16); the system comprising:

a first memory element (fig. 2: RAM 106) wherein the first memory element is configured to receive a plurality of first packet QoS indicators (col. 5 line 51: OC-3, OC-12 and OC-48; col. 5 lines 63-66: type or protocol), a first packet QoS field (col. 5 line 67: routing information) and a second packet QoS field (col. 6 lines 8-19 → col. 8 lines 56-65: session IDs);

a second memory element (fig. 2: RAM 112) wherein the second memory element is configured to hold a plurality of second packet QoS indicators (col. 6 lines 10-13: QoS; col. 6 line 65 – col. 7 line 2: state information);

a processor (fig. 2: QoS Processor 116) configured to receive one or more QoS commands (col. 7 lines 7-11: conclusions), wherein the one or more QoS commands, includes a plurality of third QoS indicators (col. 10 lines 1-5, 20-21 & 48-51: signatures), where the processor is configured to use an index (col. 9 lines 16-19: linked list) to search the second memory element (col. 9 lines 19-20: RAM 112), where the search is configured to return a subset of the plurality of the second QoS indicators (col. 9 lines 62-65: state of traffic flow),

where the index *may* be the first packet QoS field or the second packet QoS field (col. 6 lines 39-46: header information *may* be IP header starting byte; col. 9 lines 13-16: session ID),

where the processor is configured to create a modified data packet by determining which packet QoS fields to insert in the data packet (col. 7 line 64 – col. 8 line 6), where the determination is based on the based on the one or more QoS commands (col. 10 lines 14-20; col. 11 lines 8-14; col. 7 lines 7-17: conclusion → modification).

Yet, Maher does not expressively mention the packets are specifically VLAN packets and the first and second QoS fields are of VPRI, EXP or IPToS fields. Maher discloses the claimed invention yet not specifically a first VPRI field, first EXP field and first IPToS field. Alam teaches PRI field in a VLAN environment (col. 3 lines 43-50; col. 9 lines 13-15), an IPToS field (col. 4 lines 54-57; col. 9 lines 25-26) and an EXP field (col. 11 lines 41-44; col. 12 table 15). It would have been obvious to one of ordinary skill in the art when the invention was created to apply the fields of Alam as the QoS fields usable in Maher for convenient packet flow classification in a virtual routing environment.

Claims 2 and 56, applied to claims 1 and 55: Maher discloses the claimed invention yet not specifically a first VPRI field, first EXP field and first IPToS field. Alam teaches PRI field in a VLAN environment (col. 3 lines 43-50; col. 9 lines 13-15), an IPToS field (col. 4 lines 54-57; col. 9 lines 25-26) and an EXP field (col. 11 lines 41-44; col. 12 table 15). It would have been obvious to one of ordinary skill in the art when the invention was created to apply the fields of Alam as the QoS fields usable in Maher for convenient packet flow classification and marking in a virtual routing environment.

Claims 9 and 33, applied to claims 1 and 28: Maher discloses the claimed invention yet may not have specifically mentioned mark set provided by a *Virtual LAN* state table. Alam teaches a *virtual* routing engine comprising a routing processor (VRP ~ state table) in VLAN for classifying (marking) incoming packets (col. 3 lines 49-67). It would have been obvious to one of ordinary skill in the art when the invention was created to implement the virtual routing table of Alam to the network apparatus of Maher for routing VLAN data.

Claims 11 and 35, applied to claims 1 and 28: Maher discloses the mark set generated by receive components associated with memory elements (e.g. header processor 104 and CAM 320; col. 5 line 63 – col. 6 line 13, col. 8 lines 56-59) and based on priority for mark sets such as PST (port state table; col. 7 lines 52-59: control port manager). Yet have not *very specifically* mentioned VST (virtual state table), 802.1p, MPLS and IPToS. Alam teaches a *virtual* routing engine comprising a routing processor (VRP ~ state table) in VLAN for classifying (marking) incoming packets (col. 3 lines 49-67), MPLS, IPToS and 802.1p, which is well-known in the art for QoS at the MAC level expressed

through a three-bit priority field (col. 12 tables 13-15). It would have been obvious to one of ordinary skill in the art when the invention was created to set priority based on VST, 802.1p, MPLS and IPToS, etc. as taught by Alam and implement to the network apparatus of Maher since both inventions involve applying QoS field classification and modification of packet.

Claims 16-18 and 45-47, applied to claims 1 and 28: Maher discloses the modifying QoS fields and yet may not have specifically mentioned QoS commands to modify VPRI, EXP and IPToS fields. Alam teaches modifying VLAN PRI field (col. 9 lines 12-15: update PRI), EXP field (col. 11 lines 45-49) and IPToS field (col. 9 lines 24-26: replace IPToS field). It would have been obvious to one of ordinary skill in the art when the invention was created to modify the packet modification function of Maher to include modifying VPRI, EXP and IPToS fields as taught by Alam since both inventions involve applying QoS field classification and modification of packet.

Claim 29, applied to claim 1: Maher, modified by Alam, further mentions the first QoS field is generated by receive components (e.g. header processor 104) of a data distribution system (col. 6 lines 8-12).

Claim 31, applied to claim 28: Maher, modified by Alam, discloses the mark set generated by receive components (e.g. header processor 104; col. 5 line 63 – col. 6 line 13) of a data packet distribution system and is passed to transmit components (e.g. QoS processor 116; col. 7 line 64 – col. 8 line 2) of the data packet distribution system after the egress mark set is returned from an internal network (col. 6 lines 39-46: from internal content processor – col. 8 lines 2-6: to packet modification engine to PHY output/egress).

Claim 32, applied to claim 28: Maher, modified by Alam, teaches mark set is generated by receive components (e.g. header processor 104; col. 5 line 63 – col. 6 line 13), where addresses for the memory element are configured to correspond to the result of a search of a CAM element (col. 8 lines 56-59: CAM stores session ID which corresponds to a flow based on addresses: col. 6 lines 20-26), and where the search of the CAM element search is based on the structure of an incoming packet (col. 6 lines 14-19: attributes).

Claim 34, applied to claim 28: Maher, modified by Alam, further teaches mark set provided by a port state table (col. 7 lines 52-59: control port manager).

Claim 43, applied to claim 28: please see claim 14 rejection above.

Claim 44, applied to claim 28: please see claim 15 rejection above.

Claims 50 and 51, applied to claim 28: Maher discloses the modified data packet includes QoS fields from the second memory element (col. 6 line 65 – col. 7 line 11). Yet mark set including a mask field configured to mask the mark select field wherein the index is the masked mark select field and the index is the unmasked egress mark select field are not specifically mentioned. Alam discloses masked marked select field (col. 12 table 13 PRI mask) and unmasked egress mark select field (col. 12 table 14 TOS value, table 15 EXP value). It would have been obvious to one of ordinary skill in the art when the invention was created to use masking and unmasking for distinguishing mark select fields as taught by Alam to the marking process of Maher since both inventions involve egress selection through QoS marking.

Claims 52 and 53, applied to claim 28: Maher discloses the claimed invention (see claims 50-51 rejection), yet it is not expressively mentioned wherein the QoS fields

from the first memory element are used unless the third QoS fields include replacement fields. Alam teaches a concept of replacement of QoS fields by fetching from a memory element in order to support a certain destination requirement (col. 9 lines 12-33); therefore, if the destination requires no change of the packet format, there will be no need for replacement of QoS field and an original QoS field would be maintained. It would have been obvious to one of ordinary skill in the art when the invention was created to allow QoS field replacement as taught by Alam to the QoS marking function of Maher to realize the benefit of minimizing format error when transmitting the packet to a destination with a particular QoS requirement (col. 9 lines 34-37).

Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, “Maher”) in view of Wakayama et al (US 2006/0034292 A1, “Wakayama”).

Claims 6 and 13, applied to claim 1: Maher discloses the claimed invention yet may not have specifically mentioned three bits for QoS fields. Wakayama teaches a 3-bit user priority tag (marking / selecting) control that sets a QoS value ([0024]). It would have been obvious to one of ordinary skill in the art when the invention was created to use three-bit format for QoS marking as taught by Wakayama to the bit checking process of Maher since the three-bit tag is associated with VLAN and IP/MPLS header formats.

Claims 12, 30 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, “Maher”) in view of Alam (US 7340535 B1), applied to claims 1 and 28, and in further view of Wakayama et al (US 2006/0034292 A1, “Wakayama”).

Claims 12, 30 and 36, applied to claims 1 and 28: Maher discloses the claimed invention yet may not have specifically mentioned the mark set includes three QoS masks and three QoS indicators. Alam discloses *three QoS mask bits* for EXP and VPRI (e.g. col. 12 table 13: bits 22:20 PRI mask; col. 12 table 15: bits 11:9 EXP mask). It would have been obvious to one of ordinary skill in the art when the invention was created to apply the three-bit masking taught by Alam to the bit checking process of Maher since they are dealing with IP/MPLS packet formats. Yet, the exact three indicators (bits) for mark selection have not been expressively mentioned. Wakayama teaches a 3-bit user priority tag (marking / selecting) control that sets a QoS value ([0024]). It would have been obvious to one of ordinary skill in the art when the invention was created to use three-bit format for QoS marking as taught by Wakayama to the bit checking process of Maher, modified by Alam, since the three-bit tag is associated with VLAN and IP/MPLS header formats.

Claims 19, 20, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, “Maher”) in view of Alam (US 7340535 B1), applied to claims 1 and 28, and in further view of Lee (US 2003/0126286 A1).

Claims 19, 20, 47 and 48, applied to claims 1 and 28: Maher, modified by Alam, disclose the index may be of queue number or egress mark set (col. 8 lines 56-65, col. 9 lines 13-16: session ID for queue flow; col. 8 lines 51-56, col. 9 lines 16-19: linked list to egress queuing). Yet, it is not specifically mentioned that the QoS commands instructs the processor to use QoS fields from the first memory unless the search of the second memory returns QoS fields. Lee teaches a packet is checked for a first QoS requirement ([0050]) and will use a first QoS field tag if the packet is of the first QoS requirement and be loaded into a first equipment ([0051-52]); if not, then a second QoS field is applied by another upper layer equipment ([0055-56]); therefore, such may be interpreted as using a first memory element (equipment) unless a second memory (equipment) is determined (*abstract*). It would have been obvious to one of ordinary skill in the art at the time the invention was created to implement the QoS determination function of Lee to the invention of Maher, modified by Alam, for realizing multiple level priority (QoS) support.

Claims 21 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, “Maher”) in view of Alam (US 7340535 B1), applied to claims 1 and 28, and in further view of Valenci (US 2003/0185220 A1).

Claims 21 and 54, applied to claims 1 and 28: Maher, modified by Alam, discloses the claimed invention yet may not have mentioned selecting a parser generated page based on a VLAN service. Valenci discloses parsing a packet in a VLAN environment, stripping the VLAN tag and splitting data of the packet on page

(page selection) aligned buffers ([0031]). It would have been obvious to one of ordinary skill in the art when the invention was created to implement a parser generated page as taught by Valenci to the network apparatus of Maher, modified by Alam, to realize the benefit of being able to manipulate packets based on dynamic rules change applied to a parser.

Claims 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, “Maher”) in view of West et al (US 7006438 B2, “West”).

Claims 25 and 27, applied to claim 23: Maher discloses the claimed invention yet may not have specifically mentioned utilizing (host) ingress QoS indicator as an *ingress queue select* (for a host). West teaches incoming data are categorized into three ingress traffic categories (ITCs = QoS indicators) wherein the ITCs help select a queue which the data is going to (col. 5 lines 25-54; fig. 3). It would have been obvious to one of ordinary skill in the art when the invention was created to utilize multiple ingress queue to categorize each QoS level of data before further processing happens as taught by West into the network apparatus ingress of Maher to realize the benefit of reducing resource use later in the QoS processing.

Claims 37, 38, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, “Maher”) in view of Alam (US

7340535 B1), applied to claim 28, and in further view of Natarajan et al (US 2005/0149633 A1, “Natarajan”).

Claim 37, applied to claim 28: Maher, modified by Alam, discloses the claimed invention yet may not have specifically mentioned the mark set consists of *six bits*. Natarajan discloses six bits for tagging for QoS purposes ([0017]). It would have been obvious to one of ordinary skill in the art when the invention was created to utilize six bits for marking as taught by Natarajan to the bit checking process of Maher, modified by Alam, since both inventions involve applying QoS (e.g. IPToS) field classification and modification of packet.

Claims 38, 40 and 41, applied to claim 28: Maher, modified by Alam, discloses *three QoS mask bits* for EXP and VPRI (Alam – col. 12 table 13: bits 22:20 PRI mask; col. 12 table 15: bits 11:9 EXP mask). Yet, they may not have specifically mentioned the mark set consists of total *six bits*. Natarajan discloses six bits for tagging for QoS purposes ([0017]). It would have been obvious to one of ordinary skill in the art when the invention was created to utilize six bits for marking as taught by Natarajan to the bit checking process of Maher, modified by Alam, since both inventions involve applying QoS (e.g. IPToS) field classification and modification of packet.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, “Maher”) in view of Alam (US 7340535 B1), applied to claim 28, and in further view of Natarajan et al (US 2005/0149633 A1, “Natarajan”) and Wakayama et al (US 2006/0034292 A1, “Wakayama”).

Claim 39, applied to claim 28: Maher, modified by Alam, discloses the claimed invention yet may not have specifically mentioned a total of six bits for mark set wherein three of the bits provide mark selection. Natarajan discloses six bits for tagging for QoS purposes ([0017]). It would have been obvious to one of ordinary skill in the art when the invention was created to utilize six bits for marking as taught by Natarajan to the bit checking process of Maher, modified by Alam, since both inventions involve applying QoS (e.g. IPToS) field classification and modification of packet. Yet, the exact three bits for mark selection has not been expressively mentioned. Wakayama teaches a 3-bit user priority tag (marking) control that sets a QoS value ([0024]). It would have been obvious to one of ordinary skill in the art when the invention was created to use three-bit format for QoS marking as taught by Wakayama to the bit checking process of Maher, modified by Alam and Natarajan, since the three-bit tag is associated with VLAN and IP/MPLS header formats.

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al (US 6381242 B1, “Maher”) in view of Alam (US 7340535 B1), applied to claim 28, and in further view of Natarajan et al (US 2005/0149633 A1, “Natarajan”) and Colley et al (US 6650644 B1, “Colley”).

Claim 42, applied to claim 28: Maher, modified by Alam, disclose IPToS masking (Alam: col. 12 table 4), yet may not have specifically mentioned a total of six bits for mark set wherein *three* of the bits IPToS provide mark selection. Natarajan discloses six bits for tagging for QoS purposes ([0017]). It would have been obvious to one of ordinary skill

in the art when the invention was created to utilize six bits for marking as taught by Natarajan to the bit checking process of Maher, modified by Alam, since both inventions involve applying QoS field classification and modification of packet. Yet, three-bits for IPToS masking is not specifically taught. Colley teaches three-bits ToS segment in a QoS value for masking (col. 6 lines 4-8). It would have been obvious to one of ordinary skill in the art when the invention was created to modify the number of ToS bits for masking (by three bits) as taught by Colley and apply it to the bit checking process of Maher, modified by Alam and Natarajan, since both inventions involve applying QoS (e.g. IPToS) field classification and modification of packet.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Santiago et al, US 7042848 B2: hierarchical traffic flow policing system comprising parsing means, packet editing means and CAM for index search regarding packet classification
2. Paatela et al, US 2002/0163935 A1: packet modification of multi-protocol, multi-flow and streaming data wherein modification is based on protocol-dependent instructions stored in a memory such as CAM or SRAM
3. Sheth et al, US 2002/0103925 A1: apparatus utilizing dynamically modifiable combination in header fields of IPv4 packets wherein lookup module is a CAM element

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is 571-270-1780. The examiner can normally be reached on Monday through Friday 8:30 am - 6:00 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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10th October 2008

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